Electronics – II
Basics of Computer Organization
[CORE COURSE]

Semester: II	Credits:2	Subject Code: BS22008	Lectures: 40

Course Outcomes:

At the end of this course, the learner will be able to:

- Analyze, design and implement sequential logic circuit.
- Classify different semiconductor memories; Recognize the principal memory technologies from a hierarchical view point with emphasis on cache memory.
- Identify and explain different parts of CPU and I/O devices, organize them according to their function.

Unit 1: Sequential Circuits	18
• Flip flops: RS using NAND gate, clocked RS Flip-flop, J-K, Delay (D) and Toggle (T). • 3-bit Asynchronous Up and Down Counter with timing diagrams. • Concept of excitation table and state table • Design of 3-bit synchronous up counter and down counter. • Modulus of counters, Decade counters. • Ring counter, with appropriate timing diagrams, • Shift registers: SISO, SIPO, PISO, PIPO shift registers, universal 4-bit shift register and Applications.	

Unit 2: Memory Organization	10
• Classification of memory (semiconductor), Memory Parameters (Access time, capacity, cost), Memory Architecture, • Static RAM cell and Dynamic RAM cell, Diode Matrix ROM, Flash Memory. • Vertical and Horizontal Memory Expansion • Memory hierarchy, Role of Cache Memory, concept of Virtual Memory	

Unit 3: Basics of Computer System	12
• Block diagram of computer system, Concept of Address Bus, Data Bus, Control Bus • CPU block diagram and explanation of each block • General register organization, Concept of memory and register stack and its organization, SCSI • I/O organization, Need of I/O interface, block diagram of general I/O Interface.	

Board Of Studies	Name	Signature
Chairman (HoD)	Swatee Sarwate	Swatee Sarwate

Basic Reading:

- Floyd T.M.,Jain R.P ,*Digital Fundamentals*: Pearson Education
- M.Morris Mano ,*Computer System Architecture*, Pearson Education

Reference Books:

- Jain R.P., *Digital Electronics*: Tata McGraw Hill
- Malvino Leach,*Digital Principles and Applications*, Tata McGraw-Hill.
- William Stallings ,*Computer Organization and Architecture*, William Stallings,Prentice Hall India

Websites:

- https://www.csun.edu/~rd436460/DigitalElectronics/Chapter%205.pdf
- https://computer.howstuffworks.com/computer-memory2.htm
- https://en.wikipedia.org/wiki/Memory_address
- https://www.geeksforgeeks.org/introduction-of-general-register-based-cpu-organization/

E-Resources:

- NPTEL lecture series- Electronics-Digital Circuits and Systems by Prof. S. Srinivasan IITMadras, - 16 to 26 on YouTube
- https://www.youtube.com/watch?v=m1QBxTeVaNs Difference between FF & latch
- YouTube video on horizontal and vertical memory expansion https://www.youtube.com/watch?v=iyTxhDPPBXA

Contact Hours: 12 hours for Library work, practical or field work or research purposes

Board Of Studies	Name	Signature (in white cell)	
Chairman (HoD)	Swatee Sarwate	Swatee Sarwate 22/7/20	
Subject Expert (Internal)	Anitha Menon		R.A.M 22/7/20
Subject Expert (Outside SPPU)	Dr. R.K.Kamat	R.K.Kamat 22/7/20	
Subject Expert (Outside SPPU)	Dr. Sangeeta Kale		Skale 22/7/20
VC Nominee (SPPU)	Dr. Neha Deshpande	Neha Deshpande 22/7/20	
Industry Expert	Amber Mukherjee		Amber Mukherjee 22/7/20
Alumni	Supriya Palande	Palande 22/7/20	Palande

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